ABSTRACT OF THE DISCLOSURE

The present invention introduces an integrated analog multiplier-divider circuit. The multiplier-divider block according to the present invention is ideal for use in the power factor correction (PFC) controllers of many switch-mode power supplies. The analog multiplier-divider according to the present invention is built with CMOS devices. Because of this, it has many advantages over prior-art multiplier-dividers. One important advantage is that the die-size and the cost can be reduced. Another important advantage of the multiplier-divider according to the present invention is substantially reduced temperature dependence.